

A Color Television Interface

Easy — Versatile — Inexpensive

By William Rogers

The contents of this application note will cover many topics concerning the Video Display Generator; generalizing on some, baiting with others and specifying one complete project. First, I'll talk about why a versatile system is easy to build inexpensively. Then I'll turn to the performance abilities of the VDG and then mention two systems on either extreme. Fourth I'll enter into a software section including a demonstrating program, an expandable TV output display program (for an existing terminal) and a cursor program, which is the main software in this article, and is also expandable. Fifth comes the hardware section complete with an operational schematic for an Exorcisor compatible board. Other systems may function with the hardware as long as the proper signals are used.

Two new products built by Motorola help comprise a display interface circuit for the 525 line black and white televisions or the NTSC (National Television Standards Committee) standard color television sets. The Video Display Generator (MC6847), the Color TV Modulator (MC1372), some memory chips and approximately twelve passive discrete components coupled with an MC6800 microprocessor, or any other MPU (Microprocessor Unit) convert the display system into an active and intelligent terminal.

The ease of interconnection becomes apparent when constructing a system. Most pins have definite connections such as the data bus, the address bus, the analog outputs, the power pins, and the clock input. When using an MPU, the data and address buses need three-state buffers between the VDG's buses. The control pins may be hardwired or logically connected in some fashion making the degree of construction difficulty user definable. A pin similar to a memory chip's select allows three stating of the VDG's address bus and therefore accessibility to the display RAM by an MPU. The other three pins would probably not be used by hobbyist or consumer products houses unless an external character generator was required for a more sophisticated system. An example of a higher level system, which will not be discussed in this article, is the display of apparently 6K of RAM when only 1K of RAM exists in the system. The number of chips involved is decreased significantly using the VDG, therefore making a system easier to build.

Chip count also makes a system less expensive. One VDG costs about \$19.95, one TV modulator costs about \$4.42, eight 2102 1K x 1 RAMs cost approximately \$8.00, two QUAD three-state bus transceivers cost about \$5.40, and three HEX three-state buffers cost \$5.88 which add up to \$43.65. Add a few more dollars to that cost for discretes plus miscellaneous TTL for decoding and a complete display interface with alphanumeric, dense graphics and eight-color capability is achieved for less than \$50 on a single unit basis. Compared to \$250 up to a \$580 cost for boards and compared to the functionality of each board this is a substantial savings in a system investment.

*Prices given are approximations only.

Versatility? The VDG has it! Depending on how a person views the concept of modes, the VDG has eleven major modes with a total of 27 distinguishable modes including all the variations. If three state is considered as a viable mode then add one more to the total count.

An explanation of some performance abilities will also back up the variability of the VDG. The circuit operates on +5 volts only, therefore keeping system cost down if no other parts require other power supplies. An on-board character generator has 64 ASCII characters and is user definable with a mask change. An External/Internal Horizontal Synchronization and Row Preset signals are provided for the timing of an external character generator. Eight colors: magenta, blue, orange, green, cyan (a light blue color), yellow, red and buff (an off-white looking color) plus black make up the color selection. The color information feeds into the modulator from two chrominance pins R-Y (ϕA) and B-Y (ϕB). The complete video information (synchronization pulses and data) for a black and white television set comes out on the luminance pin (Y). Eight control pins allow hardware or logic selectable modes.

The first major eleven modes is an Alphanumeric mode which can use the internal or external ROM (character generator) in either green or orange color and can use inverse or noninverse video. Inverse and noninverse simply refer to the characters being black on a colored background or colored on a black background. The screen is sectioned off into 32 characters by 16 character rows.

The second mode is Semigraphic-4. This mode has a choice of eight colors or black and is alphanumeric compatible. The compatibility in this case means the SG-4 mode requires the same amount of display RAM (512 bytes) and each byte or character fills up the same amount of display area on the television screen. In other words, an alphanumeric "A" could have that same area cut up into four blocks with any combination of those blocks lit up. The color choice is one color per character or memory location or byte depending on how you care to define the information.

Semigraphics-6 is the third mode and is basically the same as SG-4 except the blocks are cut up into six pieces and a choice of two four color sets must be made with the Color Set Select pin on the VDG.

The next eight modes are referred to as full graphics modes and have increasing density and memory requirements. The memory locations relate to an area on the screen as in all other modes. The next four modes mentioned will allow a choice of two four color sets. A 64 x 64 graphics mode is three horizontal lines by four pictels or dots that the VDG lights up. This mode requires one kilobyte of memory. A 128 x 64 mode uses two dot clocks by three horizontal lines and two kilobytes of memory. A 128 x 96 graphics mode is two dot clocks wide by two horizontal lines high and uses three kilobytes of memory space. A 128 x 192 graphics

mode requires six kilobytes for a two dot clock wide by one horizontal line high display.

The following four modes only turn a pictel on or off and the on portion can be either green or white depending on the voltage applied to the Color Set Select pin. The element sizes have already been given for three of these modes but the memory requirements are different.

The 128 x 64 mode requires one kilobyte of memory. The 128 x 96 mode requires 1.5 kilobytes of memory. The 128 x 192 mode requires three kilobytes of RAM. The final and most dense mode is the 256 x 192 graphics mode and requires six kilobytes of memory. This mode maps the memory one bit for one pictel on the television screen for a total of 49,152 bits. The density of this mode will allow development of your own alphanumeric of special characters and shapes.

For alphanumeric characters of the same size as those in the alphanumeric mode, a 5 x 7 character font, with one blank line horizontally and one blank line vertically between each character, a total of 44 characters per character row can be achieved with a total of 21 character rows. This would give an overall character font of 6 x 8. Refer to Table 1 for a breakdown of the VDG modes.

For further versatility the VDG may be purchased with the non-interlace or interlace mask option, the interlace version costing slightly more. For those unfamiliar with the term interlace, a television has a frame composed of two fields, each 262½ horizontal lines for a total of 525 lines displayed on the screen.

The first field scans from the upper left hand corner to the middle of the bottom line skipping every other line as the electron beam travels downward. The second field scans from the middle of the top line to the end of the bottom line filling in the lines the first field skipped over. The interlace version scans both fields while the non-interlace only scans every other line (basically field one).

A few reasons for the availability of the two versions to customers are: 1) the non-interlace is a steady display which has neither dot crawl nor zipper effect and does not flicker at a 30 Hz rate, but scans at a 60 Hz rate allowing for an almost unperceivable screen refresh; 2) the interlace version fills in between the lines resulting in a "fuller" or more complete looking picture; 3) by separation and synchronization of odd and even fields through some external circuitry, it is possible to overlay two entirely different pictures on the TV screen. An example of this would be to overlay alphanumeric characters at the bottom of the screen on newscasts or any other broadcasts in order for the deaf or hard of hearing to enjoy television programs and announcements.

The other part of the basic display circuitry is the MC1372 Color Television Video Modulator. The chip generates a composite modulated RF video signal for the television set. The modulation of channel 3 or 4 carrier waves is possible as well as the ability to accept a sound carrier.

There are a minimum of parts required to operate this device. It requires only a single 5-volt power supply and has a TTL compatible clock output (one LS-TTL load) which can have an adjustable duty cycle with the addition of a 10K ohm potentiometer on pin 3 between supply and ground. A 50% duty cycle is achieved with no connection on pin 3.

The output pulse is basically a square wave with a frequency of 3.58 MHz which is the same frequency as the chrominance subcarrier oscillator. The output clock pulse is phase shifted for feedback to the chip. The modulator output amplitude and polarity correspond to the voltage difference between the chroma bias or Color Reference pin (pin 6) and the two color pins ϕA and ϕB (pins 7 and 5). The Chroma Modulator Output (pin 8) provides the vectorial sum of ϕA and ϕB which is fed back into the Chrominance Input (pin 10) which then RF modulates the signal. The RF tank which determines the channel or RF oscillator frequency is between pins 13 and 14. The final modulated output is pin 12 and can then be interconnected to a television set.

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TYPICAL MINIMUM AND MAXIMUM SYSTEMS

The VDG, a RAM or ROM (a ROM would be preferable since no MPU is around to store display data), and the linear modulator make a complete display system. Refer to Figure 1 for a basic display block diagram. The VDG is controlled by eight lines which may be hardwired, logically controlled through the use of TTL (Transistor Transistor Logic) and/or a PIA (Peripheral Interface Adaptor), or tied to the data lines of another block of RAM.

Before continuing, a brief explanation about the PIA is due. The MC6820 is a universal device for interfacing the MPU to peripheral instruments and equipment such as terminals, printers, cassette decks, keyboards, etc. with no or minimal external logic through two 8-bit bidirectional peripheral data buses and four handshake control lines.

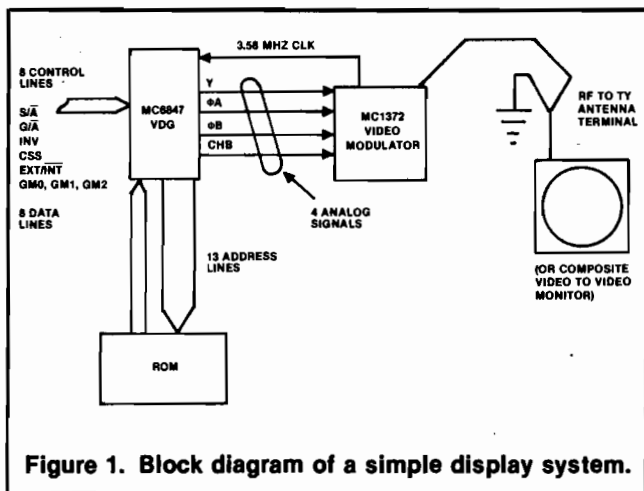


Figure 1. Block diagram of a simple display system.

During system initialization each of the sixteen data lines may be individually programmed as an input or output with a number of variations available for the type of handshake, control, or interrupt needed. A brief discussion of the above VDG control methods will be discussed shortly. The VDG increments through the address bus to the display RAM or ROM. The memory in turn outputs data to the VDG which interprets each byte according to the input on the control lines. The VDG outputs the video information on one pin and the chrominance information on two other pins.

Sync 1.0V

Blank 0.75V

Black 0.7V

White Low 0.62V

White Medium 0.5V

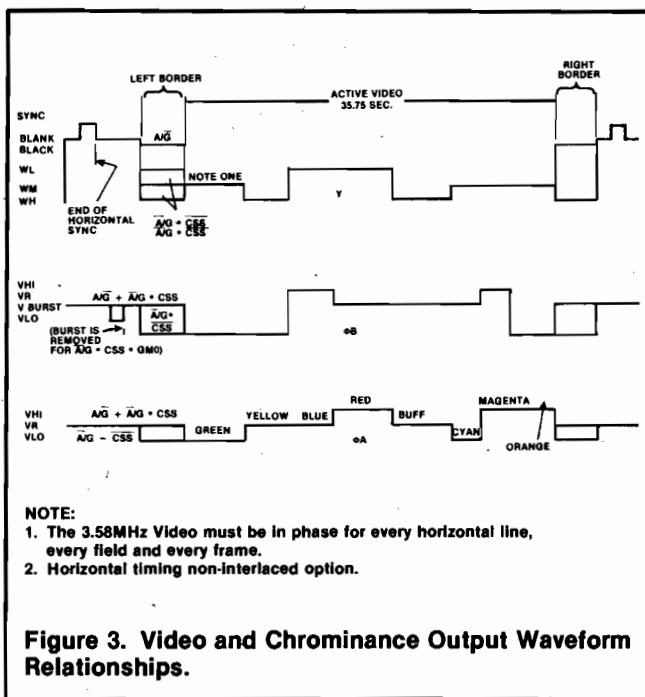
White High 0.38V

Figure 2. Nominal Luminance Levels.

(See Figure 2 for nominal luminance levels; see Figures 3 and 4 for horizontal and vertical output waveforms from the VDG.) The MC1372 modulator puts out the needed RF to the antenna terminals of a color or black and white television set. The outputs of the VDG feed into the RF oscillator modulator, which not only develops the RF carrier and final composite video signal complete with color burst, but also generates a 3.58 MHz crystal controlled clock for the VDG.

Table 2. Recommended Chroma-Luma Signals

	Pin #9 Luminance Input (Vdc)	Pin #7 Color A (Vdc)	Pin #6 Color Ref. (Vdc)	Pin #5 Color B (Vdc)
Sync	1.0	1.5	1.5	1.5
Blanking	0.75	1.5	1.5	1.5
Burst	0.75	1.5	1.5	1.25
Black	0.70	1.5	1.5	1.5
Green	0.50	1.0	1.5	1.0
Yellow	0.38	1.5	1.5	1.0
Blue	0.62	1.5	1.5	2.0
Red	0.62	2.0	1.5	1.5
Cyan	0.50	1.0	1.5	1.5
Magenta	0.50	2.0	1.5	2.0
Orange	0.50	2.0	1.5	1.0
Buff	0.38	1.5	1.5	1.5



NOTE:

1. The 3.58MHz Video must be in phase for every horizontal line, every field and every frame.
2. Horizontal timing non-interlaced option.

Figure 3. Video and Chrominance Output Waveform Relationships.

Refer to Table 2 for nominal chroma and luma input signals to the MC1372.

Now for a brief discussion on control methods. Hardwiring the control lines or using switches will allow manual operational control. The use of TTL or a PIA enables the user to switch modes on the fly under software control. This method must be under constant supervision of the MPU. The third method involves using twice as much RAM. Control RAM uses 8 bits and display data uses 8 bits (Figure 5). The MPU accesses two blocks of RAM, each 6K by 8 of bits making the available RAM look like 21K by 8 bits.

The software will initially have to know where mode information goes with respect to the display data. When the MPU is through reading and/or writing to the RAM, the VDG takes over and the blocks of RAM are simultaneously selectable by the VDG. This gives the MC6847 a memory block of 6K by 16 bits. This is allowing for a maximum system with a maximum amount of RAM. A reduction to 13 bits of RAM may be achieved by connecting some don't care data lines to

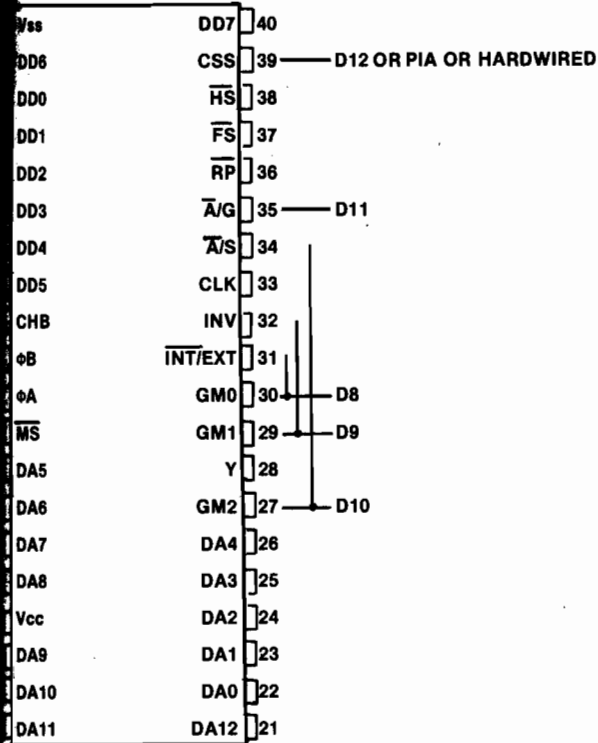


Figure 6. VDC Mode Control Connections.

Table 3. VDG Mode Selection

D ₁₁	D ₁₀	D ₉	D ₈	MODE.
0	0	0	0	Internal Alpha Numerics
0	0	0	1	External Alpha Numerics
0	0	1	0	Internal Alpha Numerics Inverted
0	0	1	1	External Alpha Numerics Inverted
0	1	X	0	Semigraphics 4
0	1	X	1	Semigraphics 6
1	0	0	0	Graphics Mode 0
1	0	0	1	Graphics Mode 1
1	0	1	0	Graphics Mode 2
1	0	1	1	Graphics Mode 3
1	1	0	0	Graphics Mode 4
1	1	0	1	Graphics Mode 5
1	1	1	0	Graphics Mode 6
1	1	1	1	Graphics Mode 7

stant supervision. The program would need to determine the number of scan lines desired in any particular mode enabling ease of mode changing, where the memory address ought to be (as far as the VDG is concerned), and if object code is used, where it is and where it ought to go in memory.

These considerations as well as general housekeeping must be taken into account by the system's microprocessor. Another way of enhancing performance with fewer parts is to use a bi-phase method. If the VDG is used with a MC6800 family microprocessor then 6K of RAM could be displayed using only 1K of actual in-system RAM.

If the Interlaced VDG is used, a flip flop could choose between memory banks of 6K each (maximum type system — less memory could be used incorporating some of the other

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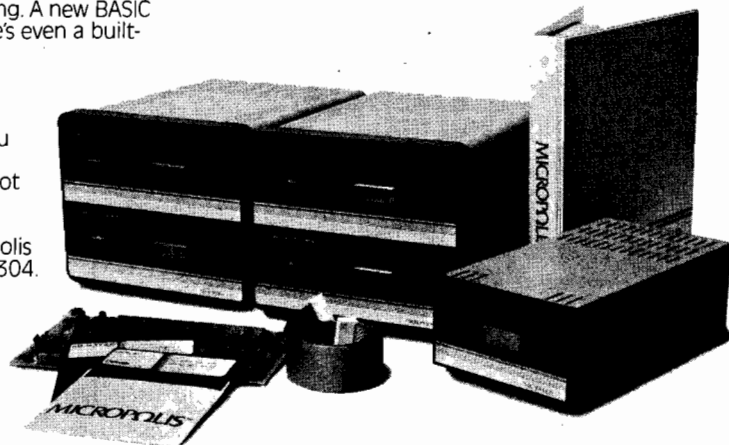
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ideas) for smaller characters on the screen since it is now effectively twice as dense as before. The flip flop is toggled by the Field Synchronization pulse enabling different information to be displayed every field change instead of having the same dot for both fields, thus allowing mapping of 98,304 bits.

SOFTWARE

Three programs are incorporated within. The first program shown in Listing 1 is extremely short and uses two modes: Alphanumerics and Semigraphics-4 mode. The data in the display memory is incremented every location to show the color and character capabilities. The alphanumerics inverted and non-inverted characters will appear first. Then two columns of four rows each with blocks of color will appear from left to right like this: green, yellow, blue, red, buff, cyan, magenta and orange. They will also appear in all the possible combinations of illumination. The VDG TEST program only loads up the display memory with successively incremented numbers and then returns control to the monitor program.

The second program shown in Listing 2 is a short piece of coding to demonstrate terminal possibilities. The program was written to run with a MIKBUG 2.0 monitor, therefore, the input routine is at \$F878. If an Exorcisor is being used, replace \$F878 with \$F015, the input without parity routine INCHNP. The program is extremely limited; it allows only alphanumeric characters (inverted and noninverted). This could use Semigraphics-4 if the user reconfigures the software for control characters putting the desired information into the display memory. In this instance the most significant bit, bit 7, indicates Alpha or Semigraphics-4.

The only special functions allowed are backspacing and escaping to the monitor. Other commands may easily be added by the user. Oddly enough the backspace key and the escape key were chosen for their respective functions. The program is not for a stand alone system; in other words the system used must already have a fully functional terminal. The program returns to the top left hand corner of the screen after the last character is input at the bottom right hand corner of the television screen.

This program may be added to quite easily. All the control characters should be checked over before any character is thrown into the display RAM and those comparisons and branches should be inserted at \$0222 between the BEQ ESC and STA A 00, X instructions. The actual code for implementation of each additional control character is placed after the ESC SWI instruction (ESC is the label and SWI is the mnemonic for the instruction Software Interrupt).

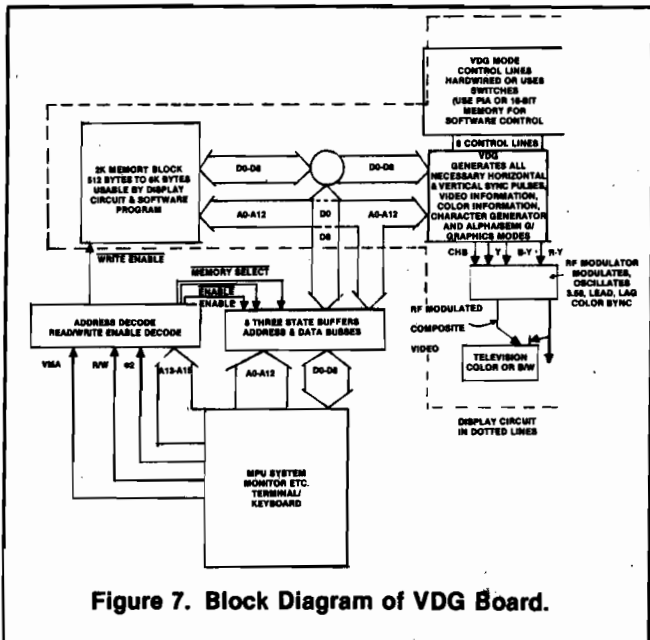


Figure 7. Block Diagram of VDG Board.

The third (and last) program is for cursor control. Again, if the Exorcisor is used change \$F878 to \$F015. The program is fairly well documented and explains itself. The cursor program assembly listing is shown in Listing 3.

The method for creating color graphics is as follows: First block off an existing picture and enlarge it on a similar screen-sized piece of graph paper. Second make a transparency of the enlarged picture and tape it over the television set. Finally use the cursor program to color in the appropriate colors behind the transparency.

HARDWARE

The system used is either an EXORCISOR or an EXORCISOR Compatible System such as a MIKBUG 2.0 controlled D2 Kit. The block diagram of the existing hardware is depicted in Figure 7. The display board interface to the Exorcisor Bus shown in Figure 8 consists of three quad three-state bus transceivers, three HEX buffers, four RAM chips (2K total), one VDG, one Linear Part and four SSI TTL logic parts for decoding. The total chip count is 16 to decode 2K bytes of static RAM and have alpha and full color graphics capability. Further decoding is possible when more RAM is desired in the system.

SWITCH SELECT FOR VDG MODES			
Switch #	VOG Pin	Function	
		INV	X X X X X X X X X X 1 0 1 0
1	30	GM0	1 0 1 0 1 0 1 0 X X X X X X
2	29	GM1	1 1 0 0 1 1 0 0 X X X X X X
3	27	GM2	1 1 1 1 0 0 0 0 X X X X X X
4	31	INT/EXT	X X X X X X X X 1 0 1 1 0 0
5	34	ALPHA/ SEMI GRAPHICS	X X X X X X X X 1 1 0 0 0 0
6	35	ALPHA/ GRAPHICS	1 1 1 1 1 1 1 1 0 0 0 0 0 0
7	39	CSS	

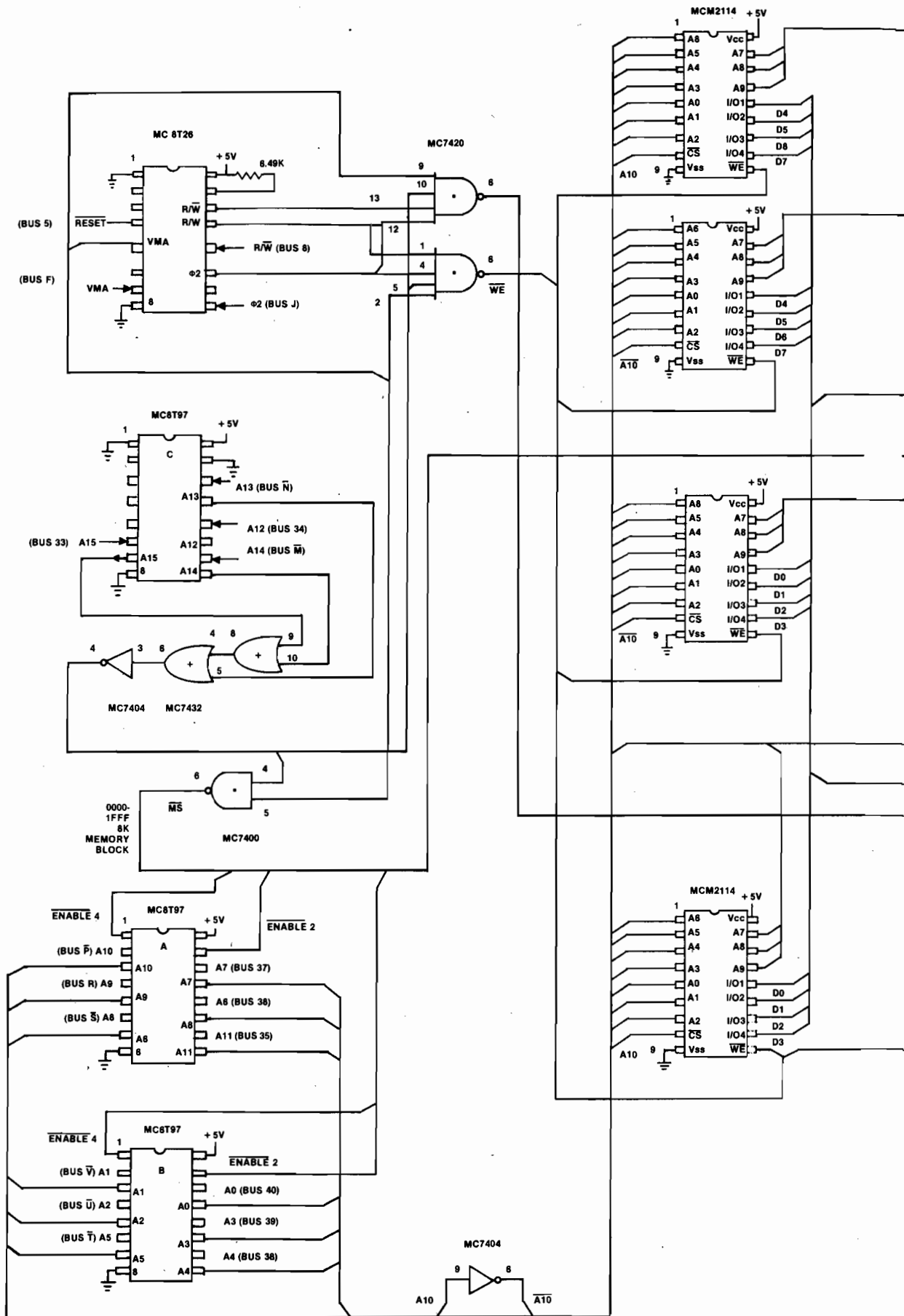
2 1 1 1 1 1 1 6 S S E E I I
5 2 2 2 2 2 2 4 E E X X N N
6 8 8 8 8 8 8 X M M T T T T
X X X X X X 6 I I
1 1 9 9 9 6 6 4 A A A A
9 9 6 6 6 4 4 G G L L L L
2 2 R R P P P P P
A A H H H H
G C G C G C G C P P A A A A
R O R O R O R O H H
A L A L A L A L I I I I
P O P O P O P O C N N
H R H R H R H R S S V V
I I I I
C G C G C G C G 6 4
S R S R S R S R
A A A A
P P P P
H H H H
I I I I
C C C C
S S S S

Figure 9. VDG Mode Switches

Note the OR gate with the output to \bar{A}/S of the VDG. This gate enables either software or hardware control of the Semigraphics modes. Software control is desired when switching between Alpha and Semigraphics-4 mode. The hardware switch input to the OR gate is to cancel out the effects of Data bit 7 on the control pins when Semigraphics-6 mode is desired. If the gate were not present the switch and resistors would conflict with the data bus bit 7 causing sections on the screen to flicker, resulting in unreliably displayed data.

All control pins (as well as the data bus) must have "solid" information on them and must not be left floating at an unknown state. Good grounding of the connectors around the RF output and shielding high frequency areas will enhance the appearance of the television display. The capacitor values around the 3.58 crystal are not extremely critical, but for individual systems a trimmer capacitor may replace the 15 pf capacitor. The mode choice, via the switches, is shown in Figure 9. □

Figures & Listings follow



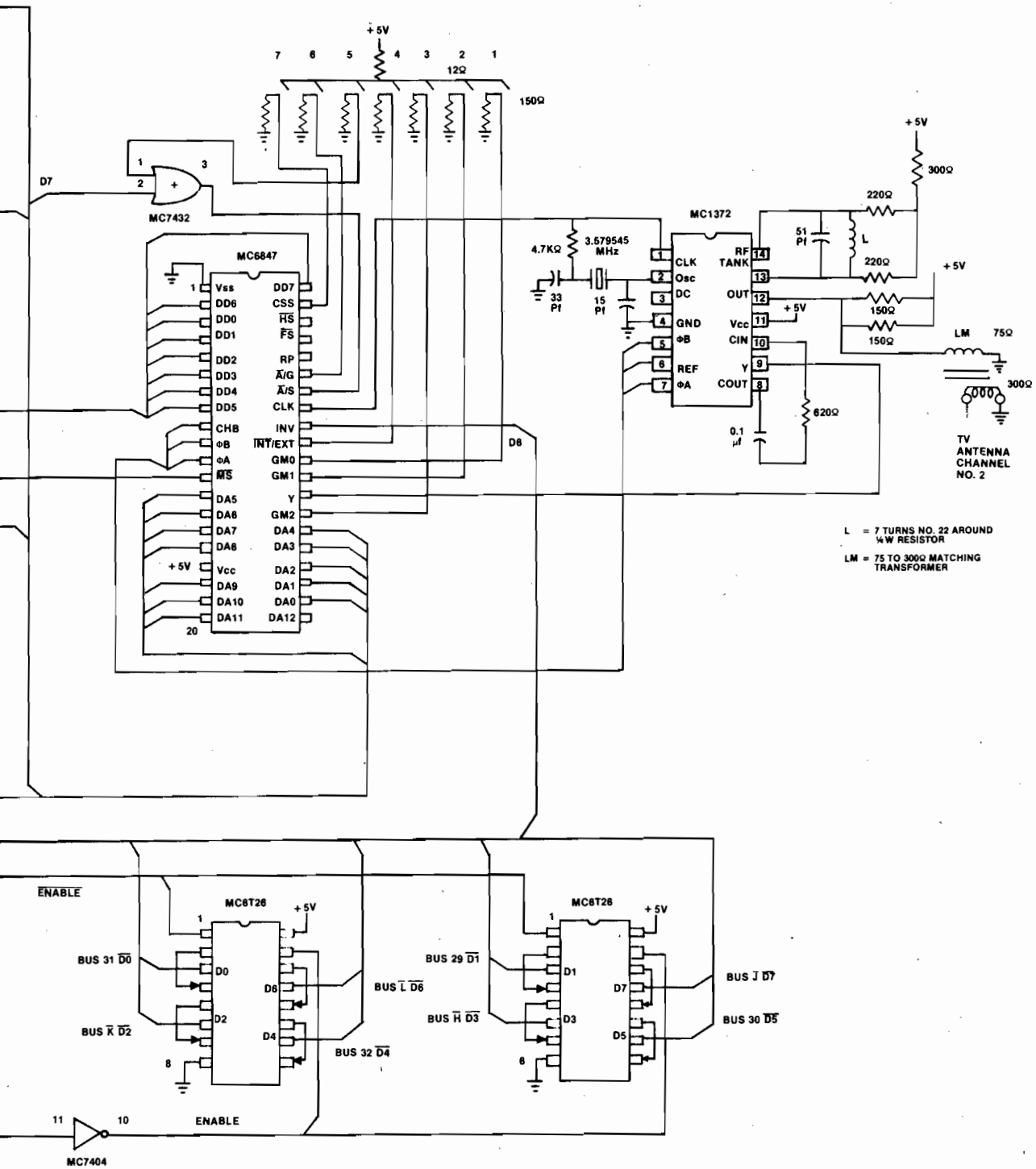


Figure 8.

LISTING 1

```

NMH VDGTEST
* THIS PROGRAM DEMONSTRATES THE ALPHANUMERICS MODE
* AND THE SEMI GRAPHICS 4 ( 8 COLORS PLUS BLACK MODE)
0210 CE 00 00 DRG #0210 BEGINNING OF DISPLAY PROGRAM
0213 B6 00 LDX #00000 START ADD OF DISPLAY IN X REG
0215 A7 00 LDA A #800 ACC A INCREMENTS DATA
0217 4C 00 STA A 00,X LDR UP DISPLAY MEMORY
0218 08 INC A NEXT PIECE OF INFO
0219 5C 00 CPX #0200 NEXT DISPLAY LOCATION
021E 03 BEB STOP ENTIRE DISPLAY FULL
021F 03 BEB STOP IF FULL THEN STOP PROG
021E 7E 0E 15 IF NOT INCREMENT DATA AND MEMORY
0221 3F SWP CNT RETURN TO MONITOR
END
NO ERROR(S) DETECTED

```

```

SYMBOL TABLE:
S1130210CE00008600R7004C08BC020027037E0253
S105020153F84S9
*
S1130210CE00008600R7004C08BC020027037E0253
S105020153F84S9
*

```

LISTING 2

```

NMH VDGHT
* THIS IS A VIDEO DISPLAY GENERATOR MINI-OUTPUT TERMINAL
* IT ACCEPTS INPUTS FROM THE TERMINAL AND DISPLAYS THE INFO
* ON THE TELEVISION SCREEN NORMALLY INVERTED FOR
* ALPHA AND NONINVERTED FOR NUMERICS AND SPECIAL CHARACTERS
* THE OTHER (INVERT OR NONINVERT) IS ACHIEVED BY
* DEPRESSING THE CONTROL KEY AND THEN THE DESIRED CHARACTER
* BEGINNING OF PROGRAM
0210 CE 00 00 START LDX #0200 BEGINNING OF SCREEN RAM
0213 B6 20 LDA H #820 LDR AN ASCII BLANK INTO ACC A
0215 A7 00 STA A 00,X DISPLAY CONTENTS OF ACC A
0217 80 F8 78 CNT JAR #F878 JUMP TO INPUT ROUTINE INCH
021A 81 08 CMP A #808 ASCII BS? BACKSPACE X REG
021C 27 0F BEQ BS IF 30 GO DECREMENT X REG
0220 27 0E BEQ ESC ASCII ESC? EXCAPE
0222 A7 00 STA H 00,X IF 30 JUMP OUT OF PROGRAM
0224 08 INK H 00,X PUT DATA IN DISPLAY
0225 9C 02 00 TOP CPX #0200 NEXT LOCATION IN DISPLAY
0228 27 E6 BEQ START HT END OF DISPLAY?
022A 7E 02 17 JMP CNT IF 30: GO TO TOP OF SCREEN
022D 09 DEB BACKSPACE BY DECREMENTING X REG
022E 20 F5 BPH TDP CONTINUE THROUGH PROGRAM
0230 3F ESC SWI RETURN TO MONITOR
END
* VDSMOT IS USABLE IN THE SEMI GRAPHICS & GRAPHICS MODES
NO ERROR(S) DETECTED

```

```

SYMBOL TABLE:
S1130210CE00008600R7000BF8788108E270F811B37
S1130220E70E7000986C020027E67E0E17092UF596
S10402303F84S9
*

```

LISTING 3

```

PAGE 001 CURSOR
00002 NMH CURSOR
00003 * THIS PROGRAM DISPLAYS A CURSOR WITH MOVEMENT AND COLOR SELECTION
00004 * THE CURSOR WILL BE IN ANY FOUR COLOR GRAPHICS MODE
00005 * IS IN ANY FOUR COLOR GRAPHICS MODE
00006 *
00007 *
00008 *
00010 * MEMORY SETUP: THERE ARE FOUR INDIVIDUAL 'CHARACTERS'
00011 * COLOR CODES INTO ONE OF FOUR CHARACTERS
00012 * WITHIN THE BLOCK OR MEMORY LOCATION EVERY TIME
00013 * COLOR INFORMATION IS INPUT FROM THE TERMINAL
00014 *
00015 * *****
00016 *

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Table with columns: Address, Symbol, Comment. Contains assembly code for LISTING 1 and LISTING 2.

00017	00018	00019	00020	00021	00022	00023	00024	00025	00026	00027	00028	00029	00030	00031	00032	00033	00034	00035	00036	00037	00038	00039	00040	00041	00042	00043	00044	00045	00046	00047	00048	00049	00050	00051	00052	00053	00054	00055	00056	00057	00058	00059	00060	00061	00062	00063	00064	00065	00066	00067	00068	00069	00070	00071	00072	00073	00074	00075	00076	00077	00078	00079	00080	00081	00082	00083	00084	00085	00086	00087	00088	00089	00090	00091	00092	00093	00094	00095	00096	00097	00098	00099	00100	00101	00102	00103	00104	00105	00106	00107	00108	00109	00110	00111	00112	00113	00114	00115	00116	00117	00118	00119	00120	00121	00122	00123	00124	00125	00126	00127	00128	00129	00130	00131	00132	00133	00134	00135	00136	00137	00138	00139	00140	00141	00142	00143	00144	00145	00146	00147	00148	00149	00150	00151	00152	00153	00154	00155	00156	00157	00158	00159	00160	00161	00162	00163	00164	00165	00166	00167	00168	00169	00170	00171	00172	00173	00174	00175	00176	00177	00178	00179	00180	00181	00182	00183	00184	00185	00186	00187	00188	00189	00190	00191	00192	00193	00194	00195	00196	00197	00198	00199	00200	00201	00202	00203	00204	00205	00206	00207	00208	00209	00210	00211	00212	00213	00214	00215	00216	00217	00218	00219	00220	00221	00222	00223	00224	00225	00226	00227	00228	00229	00230	00231	00232	00233	00234	00235	00236	00237	00238	00239	00240	00241	00242	00243	00244	00245	00246	00247	00248	00249	00250	00251	00252	00253	00254	00255	00256	00257	00258	00259	00260	00261	00262	00263	00264	00265	00266	00267	00268	00269	00270	00271	00272	00273	00274	00275	00276	00277	00278	00279	00280	00281	00282	00283	00284	00285	00286	00287	00288	00289	00290	00291	00292	00293	00294	00295	00296	00297	00298	00299	00300	00301	00302	00303	00304	00305	00306	00307	00308	00309	00310	00311	00312	00313	00314	00315	00316	00317	00318	00319	00320	00321	00322	00323	00324	00325	00326	00327	00328	00329	00330	00331	00332	00333	00334	00335	00336	00337	00338	00339	00340	00341	00342	00343	00344	00345	00346	00347	00348	00349	00350	00351	00352	00353	00354	00355	00356	00357	00358	00359	00360	00361	00362	00363	00364	00365	00366	00367	00368	00369	00370	00371	00372	00373	00374	00375	00376	00377	00378	00379	00380	00381	00382	00383	00384	00385	00386	00387	00388	00389	00390	00391	00392	00393	00394	00395	00396	00397	00398	00399	00400	00401	00402	00403	00404	00405	00406	00407	00408	00409	00410	00411	00412	00413	00414	00415	00416	00417	00418	00419	00420	00421	00422	00423	00424	00425	00426	00427	00428	00429	00430	00431	00432	00433	00434	00435	00436	00437	00438	00439	00440	00441	00442	00443	00444	00445	00446	00447	00448	00449	00450	00451	00452	00453	00454	00455	00456	00457	00458	00459	00460	00461	00462	00463	00464	00465	00466	00467	00468	00469	00470	00471	00472	00473	00474	00475	00476	00477	00478	00479	00480	00481	00482	00483	00484	00485	00486	00487	00488	00489	00490	00491	00492	00493	00494	00495	00496	00497	00498	00499	00500	00501	00502	00503	00504	00505	00506	00507	00508	00509	00510	00511	00512	00513	00514	00515	00516	00517	00518	00519	00520	00521	00522	00523	00524	00525	00526	00527	00528	00529	00530	00531	00532	00533	00534	00535	00536	00537	00538	00539	00540	00541	00542	00543	00544	00545	00546	00547	00548	00549	00550	00551	00552	00553	00554	00555	00556	00557	00558	00559	00560	00561	00562	00563	00564	00565	00566	00567	00568	00569	00570	00571	00572	00573	00574	00575	00576	00577	00578	00579	00580	00581	00582	00583	00584	00585	00586	00587	00588	00589	00590	00591	00592	00593	00594	00595	00596	00597	00598	00599	00600	00601	00602	00603	00604	00605	00606	00607	00608	00609	00610	00611	00612	00613	00614	00615	00616	00617	00618	00619	00620	00621	00622	00623	00624	00625	00626	00627	00628	00629	00630	00631	00632	00633	00634	00635	00636	00637	00638	00639	00640	00641	00642	00643	00644	00645	00646	00647	00648	00649	00650	00651	00652	00653	00654	00655	00656	00657	00658	00659	00660	00661	00662	00663	00664	00665	00666	00667	00668	00669	00670	00671	00672	00673	00674	00675	00676	00677	00678	00679	00680	00681	00682	00683	00684	00685	00686	00687	00688	00689	00690	00691	00692	00693	00694	00695	00696	00697	00698	00699	00700	00701	00702	00703	00704	00705	00706	00707	00708	00709	00710	00711	00712	00713	00714	00715	00716	00717	00718	00719	00720	00721	00722	00723	00724	00725	00726	00727	00728	00729	00730	00731	00732	00733	00734	00735	00736	00737	00738	00739	00740	00741	00742	00743	00744	00745	00746	00747	00748	00749	00750	00751	00752	00753	00754	00755	00756	00757	00758	00759	00760	00761	00762	00763	00764	00765	00766	00767	00768	00769	00770	00771	00772	00773	00774	00775	00776	00777	00778	00779	00780	00781	00782	00783	00784	00785	00786	00787	00788	00789	00790	00791	00792	00793	00794	00795	00796	00797	00798	00799	00800	00801	00802	00803	00804	00805	00806	00807	00808	00809	00810	00811	00812	00813	00814	00815	00816	00817	00818	00819	00820	00821	00822	00823	00824	00825	00826	00827	00828	00829	00830	00831	00832	00833	00834	00835	00836	00837	00838	00839	00840	00841	00842	00843	00844	00845	00846	00847	00848	00849	00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